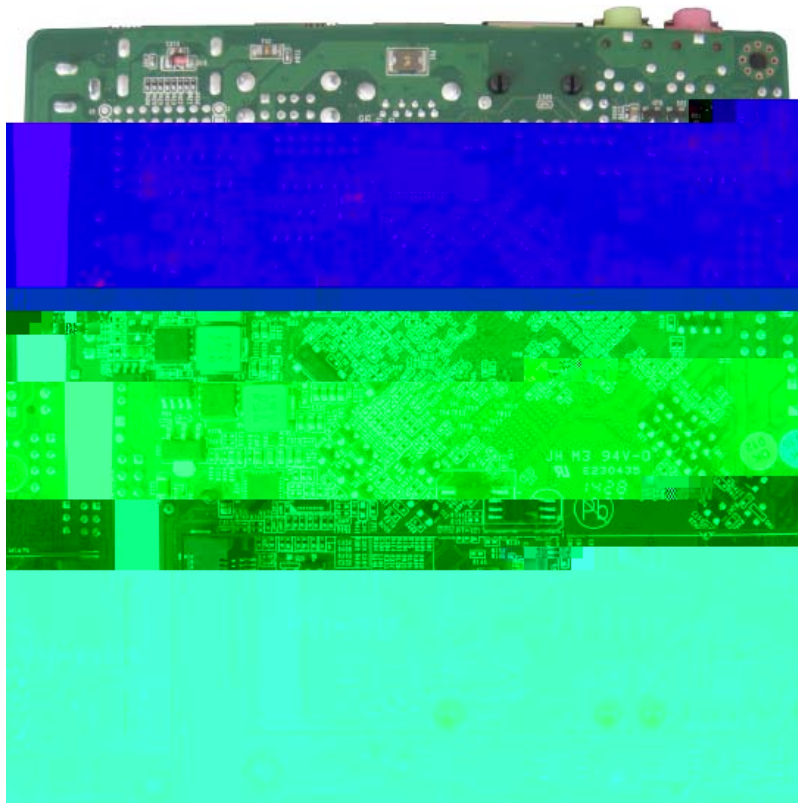
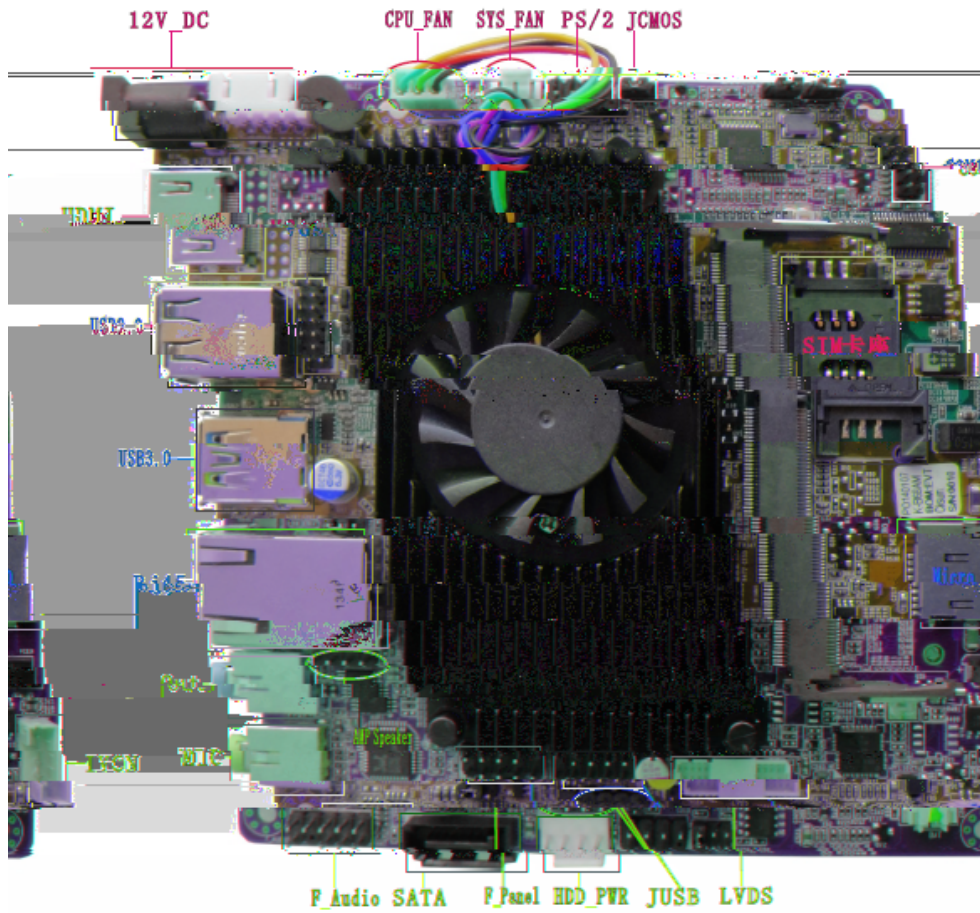
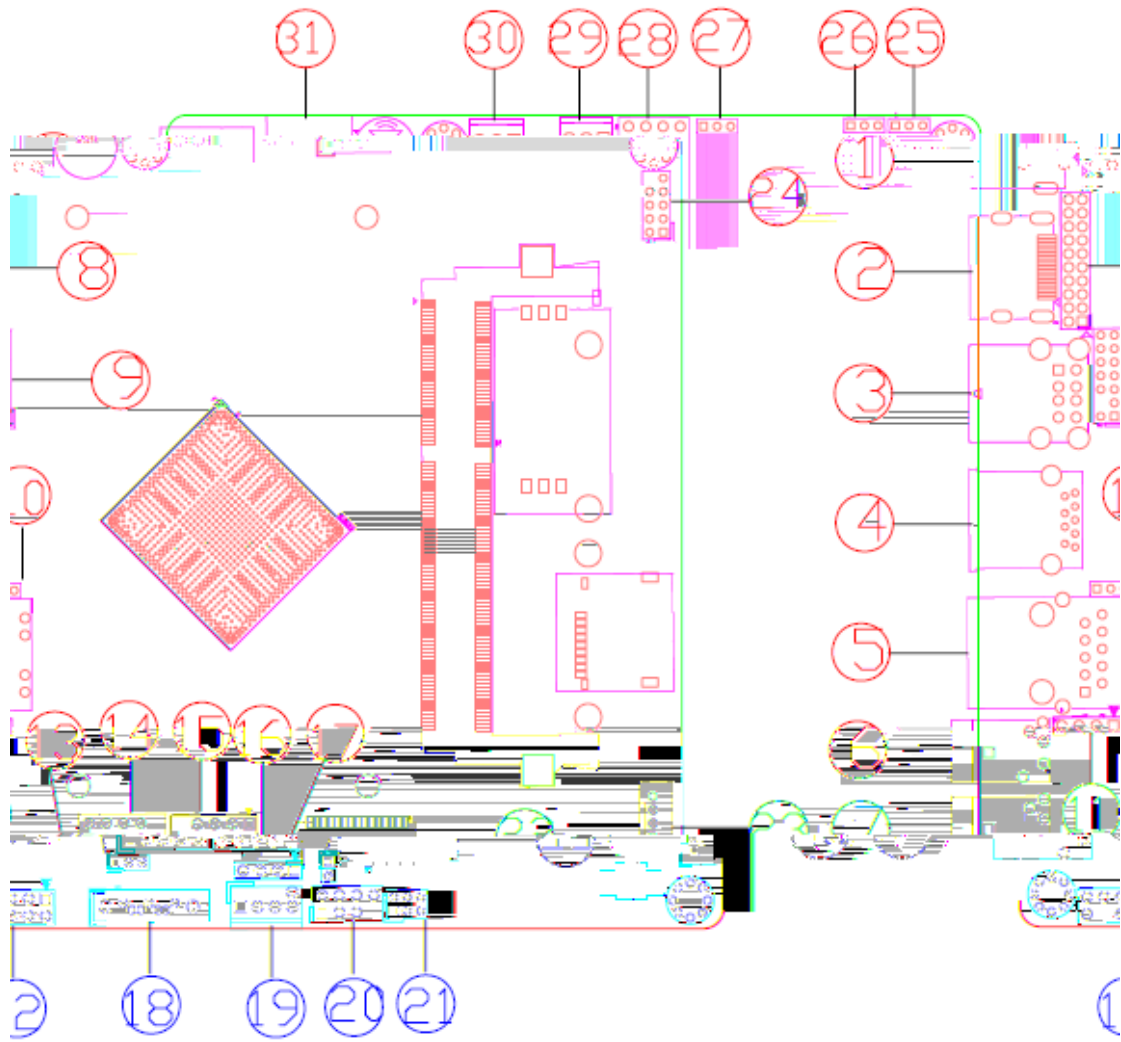






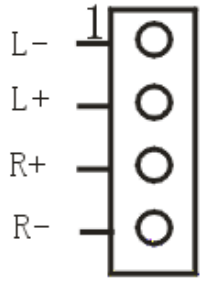
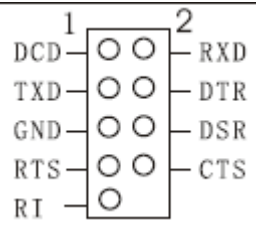
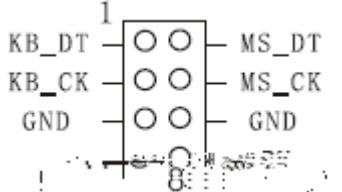
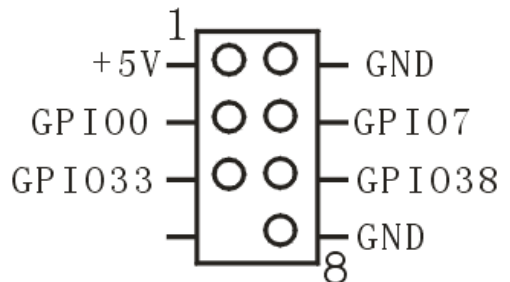
	CPU	Intel SoC Bay Trail J1800	
		2.58GHz	
		10w SMD BGA	
		SOC	
		SO-DIMM DDR3L-800/1066/1333 DDR3L-1600	
		1.35v	
		4GB	
Bios	SPI AMI EFI bios		
	ACPI2.0B, APM1.2, DIM2.0, SMBIOS2.5		
	Intel HD Graphics 311~688MHz Burst 895MHz		
	1	VGA	
	1	HDMI Port	
	1	24 LVDS	
	Realtek RTL8111E		
	10/100/1000Mbps		
	1	RJ45	
Audio	Realtek HD ALC662		
	1	Line-out,1 MIC	
	1	2 6w/8	
USB	USB3.0 2.0		
	1	USB3.0 Port 2 USB2.0 Port 2 USB	






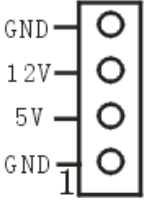
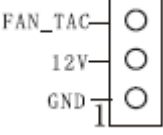
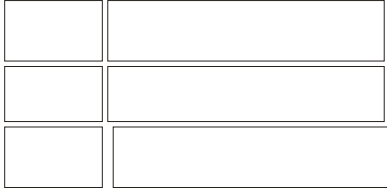
1	DC_IN	12v DC D=2.5mm
2	HDMI	HDMI
3	USB1	USB2.0
4	USB2	USB3.0
5	LAN	RJ45
6	Line-out	Line-out
7	MIC	MIC
8	JHDMI	HDMI lay HDMI
9	VGA	VGA
10	JC1	USB
11	SPEAKER	
12	F_audio	
13	AT_ATX	
14	F_PANEL	---- / HDD/PWR LED
15	JUSB1	USB 2.0
16	JUSB2	USB 2.0
17	JP1	LVDS
18	SATA	SATA
19	HDD_PWR	SATA 2.0 HDD
20	GP	
21	JC3	LVDS 12V/5V/3.3V
22	LVDS	24 LVDS
23	IVCN	LVDS Inverter
24	JCOM1	COM1
25/26	J2/J1	COM1 TTL RS232
27	JCMOS	CMOS
28	PS2	PS/2 MS KB
29	CPU_FAN	CPU
30	SYS_FAN	
31	ATX_12V	PH Wafer 1*4 4PIN 12v DC



SPEAKER																																		
VGA1	VGA	<table border="1" data-bbox="837 533 1300 929"> <thead> <tr> <th>Pin</th> <th>Signal</th> <th>Pin</th> <th>Signal</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>GND</td> <td>2</td> <td>5V</td> </tr> <tr> <td>3</td> <td>RED</td> <td>4</td> <td></td> </tr> <tr> <td>5</td> <td>GND</td> <td>6</td> <td>CLK</td> </tr> <tr> <td>7</td> <td>GREEN</td> <td>8</td> <td>DATA</td> </tr> <tr> <td>9</td> <td>GND</td> <td>10</td> <td>VSYNC</td> </tr> <tr> <td>11</td> <td>BLUE</td> <td>12</td> <td>HSYNC</td> </tr> <tr> <td>13</td> <td>GND</td> <td>14</td> <td>GND</td> </tr> </tbody> </table>	Pin	Signal	Pin	Signal	1	GND	2	5V	3	RED	4		5	GND	6	CLK	7	GREEN	8	DATA	9	GND	10	VSYNC	11	BLUE	12	HSYNC	13	GND	14	GND
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J1/J2	COM2	<table border="1" data-bbox="845 1198 1268 1321"> <tr> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> <tr> <td></td> <td></td> <td></td> </tr> </table>																																
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GP																																		



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C3	LVDS	<table border="1"> <thead> <tr> <th>设置</th> <th>说明</th> </tr> </thead> <tbody> <tr> <td>1-2</td> <td>+3.3V</td> </tr> <tr> <td>3-4</td> <td>+5V</td> </tr> <tr> <td>5-6</td> <td>+12V</td> </tr> </tbody> </table>	设置	说明	1-2	+3.3V	3-4	+5V	5-6	+12V																																																								
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HDD_PWR	HDD	
CPU_FAN SYS_FAN	FAN	
AT_ATX		

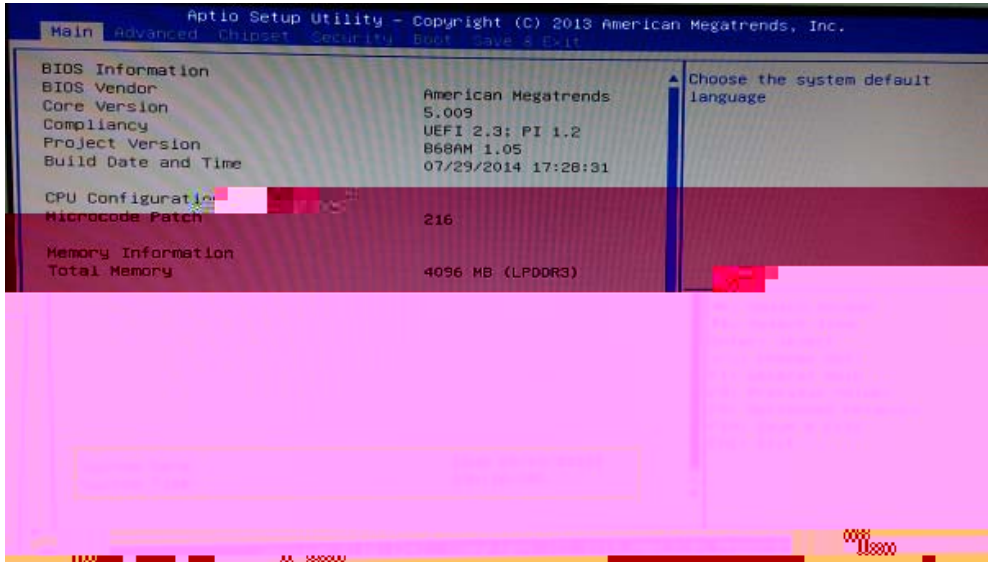
# BIOS

F2

BIOS

1

BIOS CMOS



System Time  
System Date

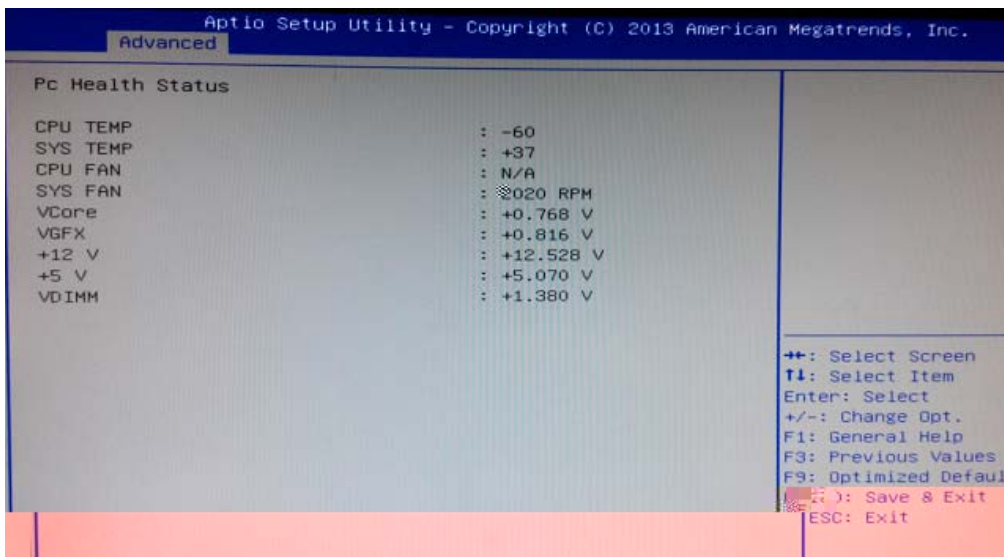
2

FAN

BIOS CMOS

"Advanced"-> IT8772E H/W

Monitor



bios

CPU

CPU

CPU

0

CPU

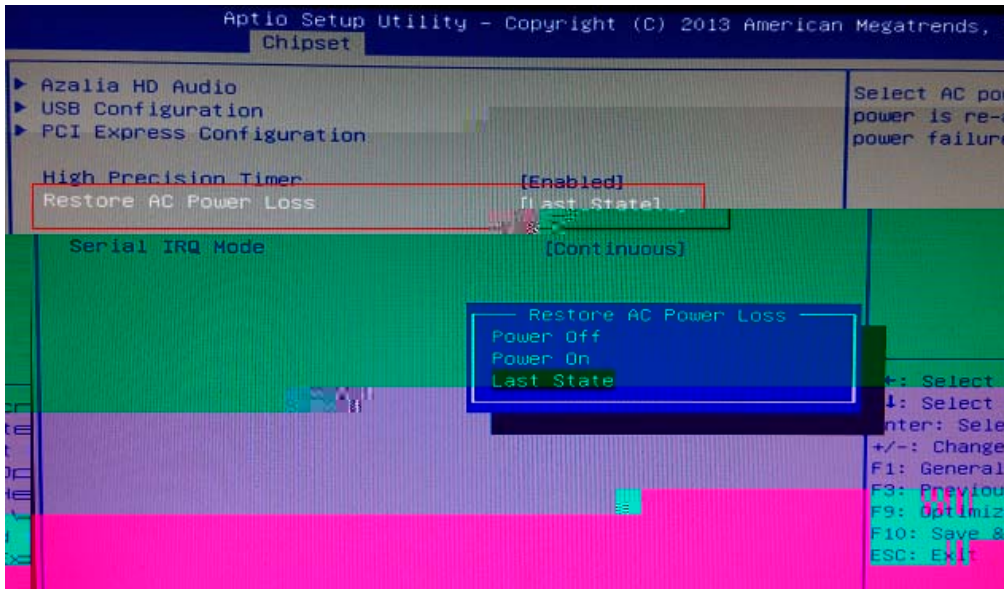
-60

CPU

60

3

"Chipset" --->"South Bridge", "Restore AC Power Loss"  
"Power ON", Power Off



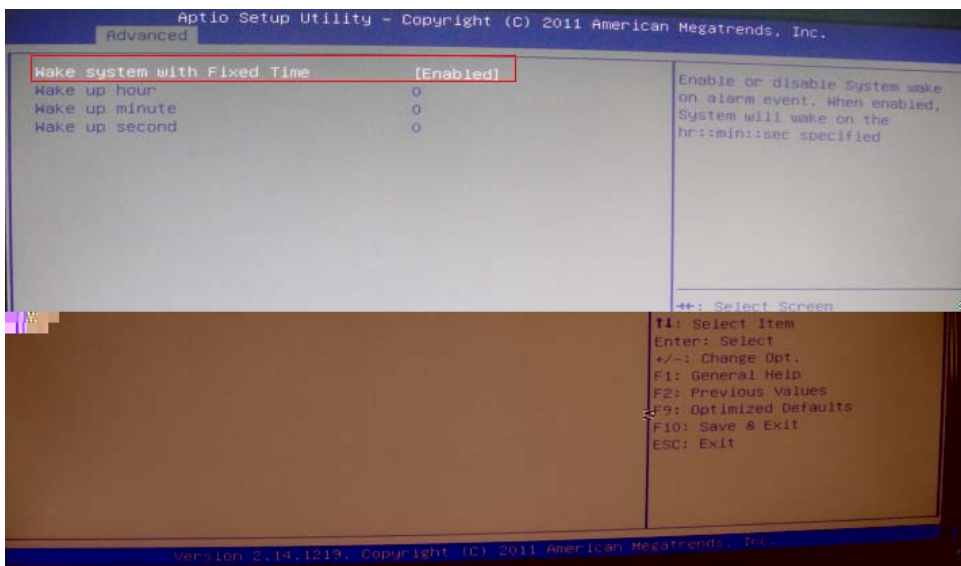
4

CMOS "Advanced"-> IT8772E H/W Monitor ,  
"Watchdog "



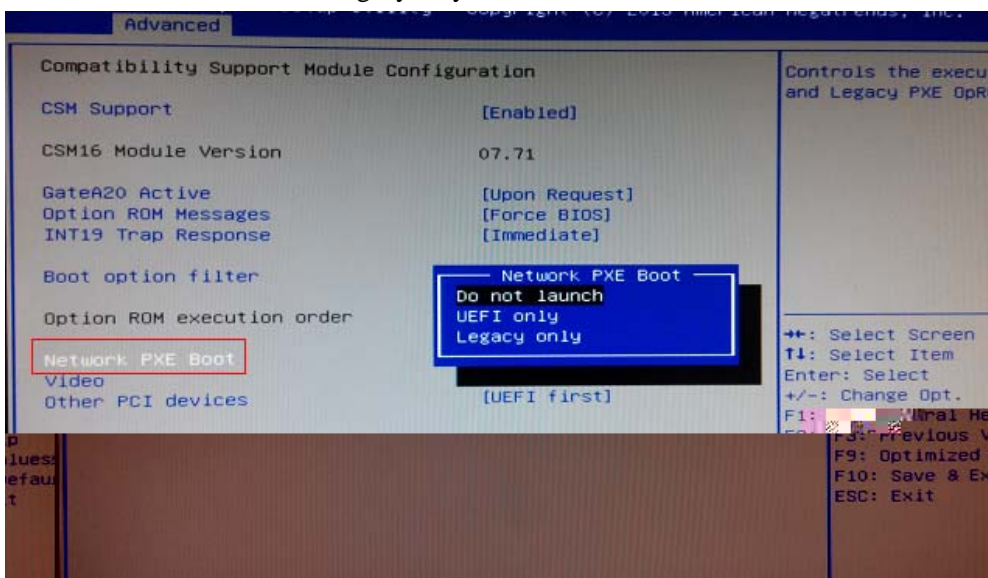
5

CMOS "Advanced"-->"S5 RTC Wake Settings"  
"disable" "Enable",  
: ok



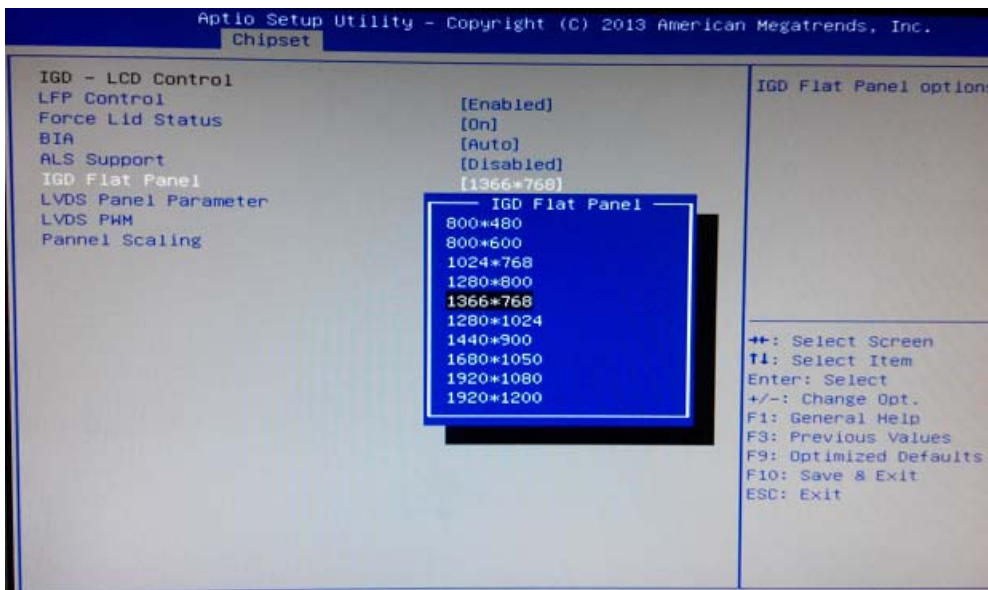
### 6 PXE

CMOS "Advanced" "CSM Configuration", Network  
 PXE Boot "Legacy only", PXE



### 7 LVDS

CMOS "Chipset"-->"Host Bridge"-->"IGD LCD Control" LCD Flat  
 Panel

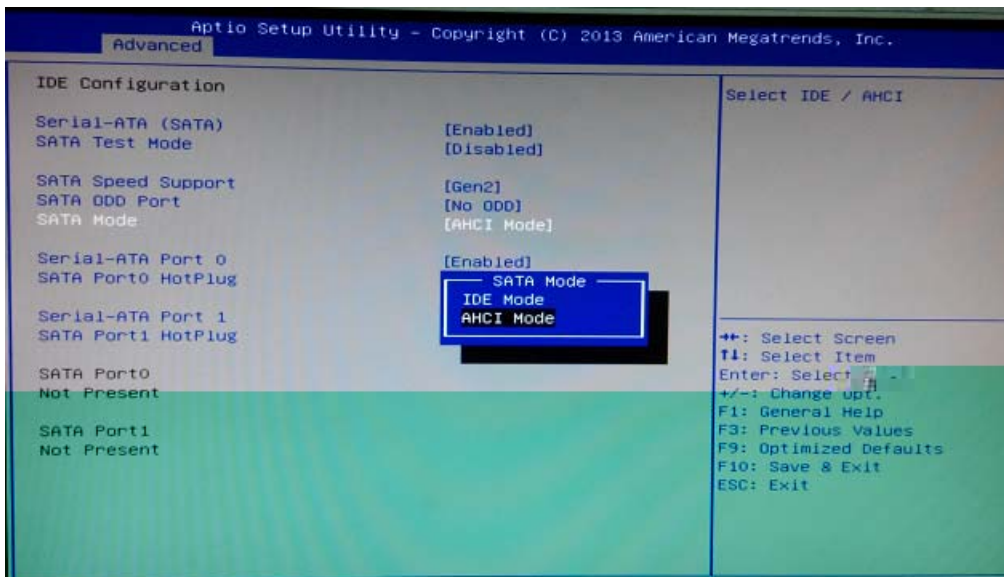


8 SATA HDD

CMOS Mode

"Chipset"--> IDE Configuration

SATA



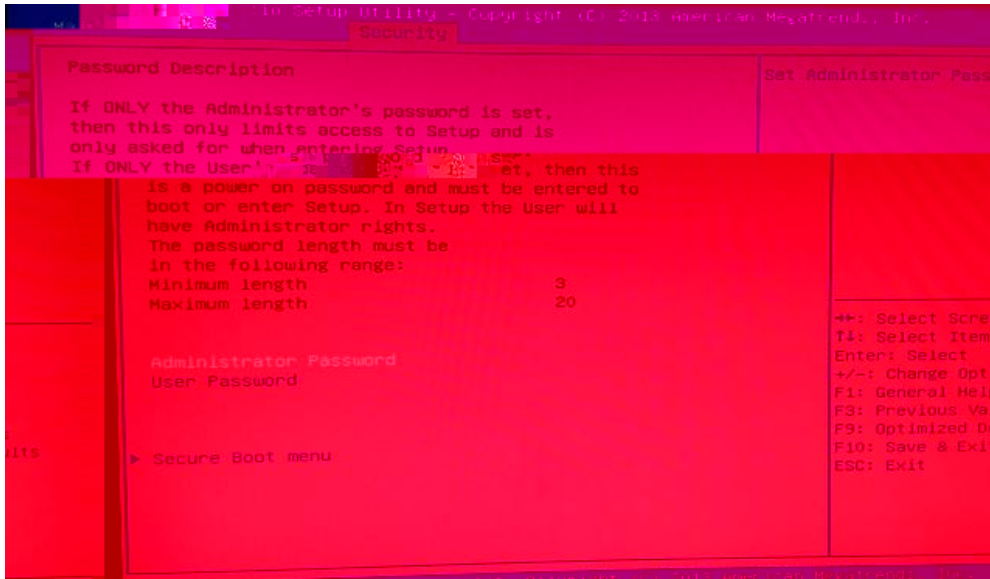
IDE AHCI

2

8

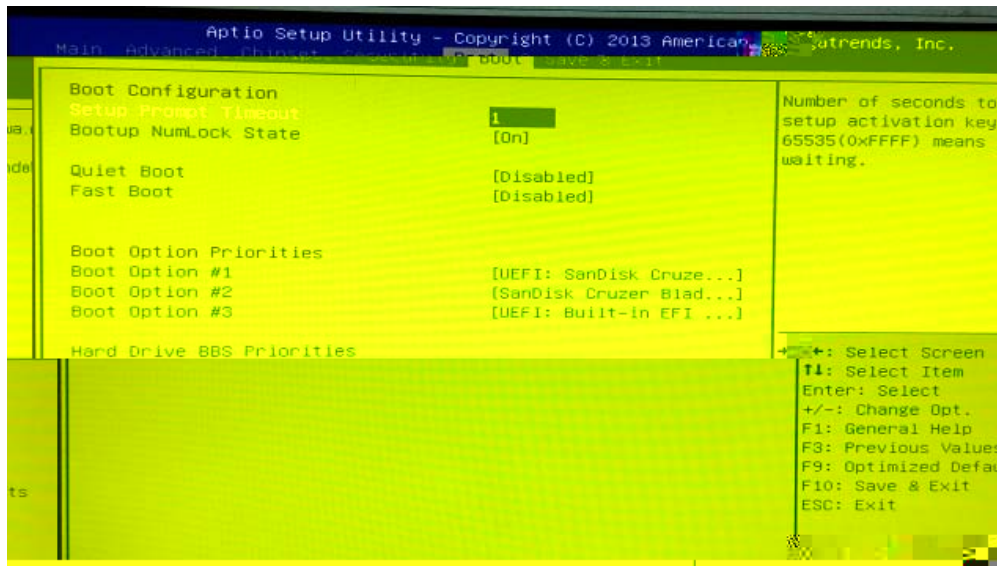
CMOS

"Security"



9 boot

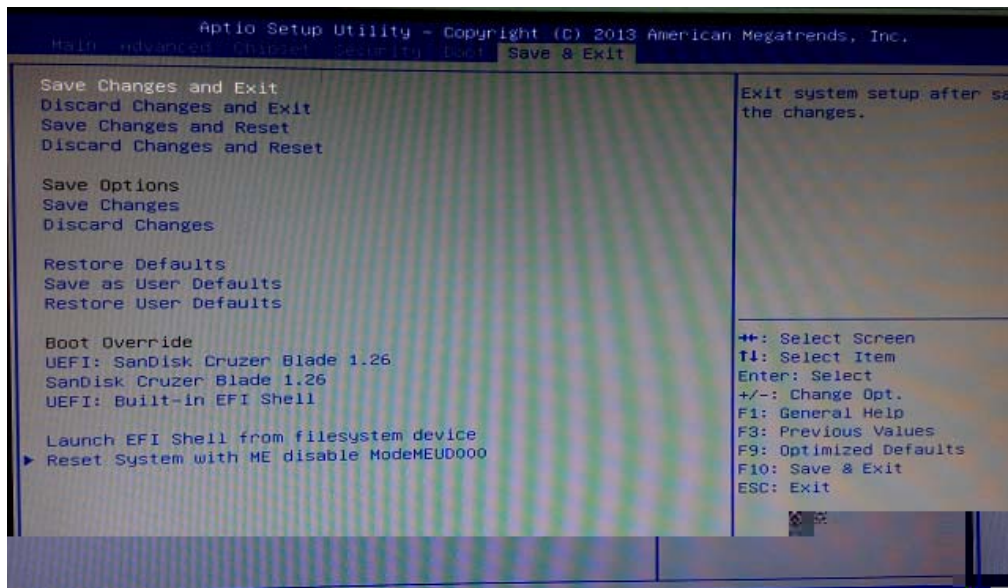
CMOS "boot"



HDD Hard Drive BBS Priorities

10

CMOS "Save&Exit"



F9

bios F10

bios.